DIGITAL ELECTRONICS LAB
(EE-224-F)

LAB MANUAL

IV SEMESTER

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LIST OF EXPERIMENTS

EXPERIMENT 1

AIM: - Introduction to Digital Electronics Lab- Nomenclature of Digital Ics , Specifications, Study of the Data Sheet, Concept of Vcc and Ground, Verification of the Truth Tables of Logic Gates using TTL Ics.

THEORETICAL CONCEPT:

AND Gate: The AND operation is defined as the output as (1) one if and only if all the inputs are (1) one. 7408 is the two Inputs AND gate IC.A&B are the Input terminals & Y is the Output terminal.

$$Y = A.B$$

OR Gate: The OR operation is defined as the output as (1) one if one or more than 0 inputs are (1) one. 7432 is the two Input OR gate IC. A&B are the input terminals & Y is the Output terminal.

$$Y = A + B$$

NOT GATE: The NOT gate is also known as Inverter. It has one input (A) & one output (Y). IC No. is 7404. Its logical equation is,

$$Y = A \text{ NOT } B, \; Y = A'$$

NAND GATE: The IC no. for NAND gate is 7400. The NOT-AND operation is known as NAND operation. If all inputs are 1 then output produced is 0. NAND gate is inverted AND gate.

$$Y = (A.\ B)'$$

NOR GATE: The NOR gate has two or more input signals but only one output signal. IC 7402 is two I/P IC. The NOT- OR operation is known as NOR operation. If all the inputs are 0 then the O/P is 1. NOR gate is inverted OR gate.

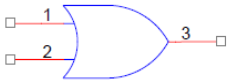
$$Y = (A+B)'$$

EX-OR GATE: The EX-OR gate can have two or more inputs but produce one output. 7486 is two inputs IC. EX-OR gate is not a basic operation & can be performed using basic gates.

$$Y = A\ B$$

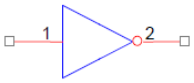
EXPERIMENTAL SET UP :

Logic Symbol of Gates



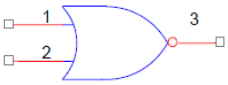
OR

AND

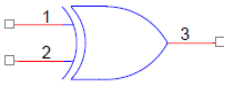


NOT

NAND



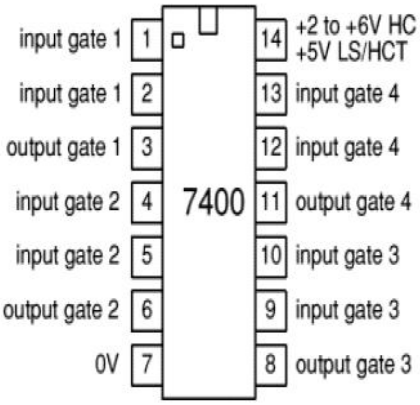
NOR



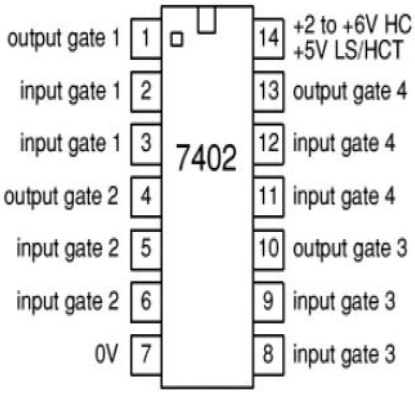
XOR

PIN CONFIGURATION:

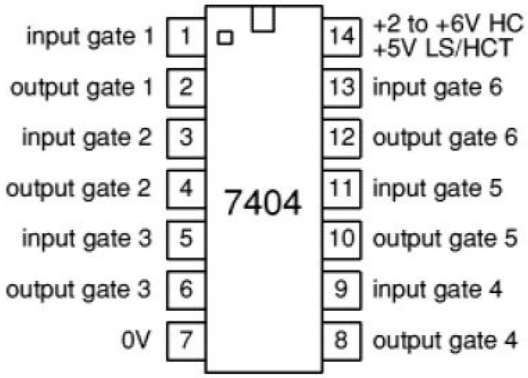
7400(NAND)



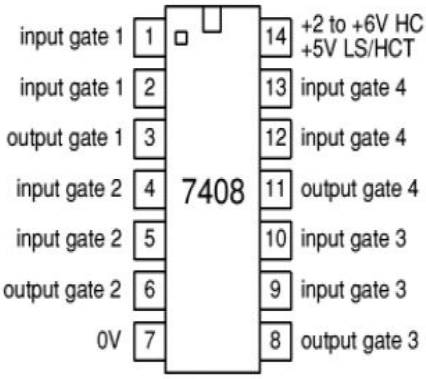
7402(NOR)



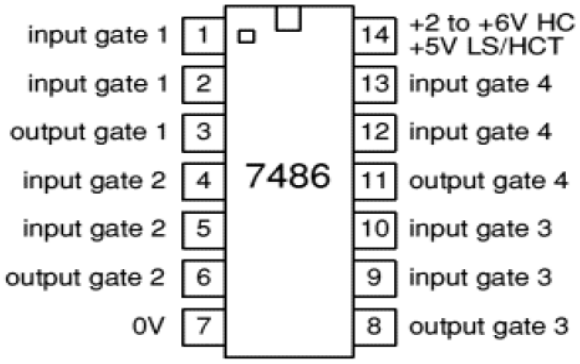
7404(NOT)



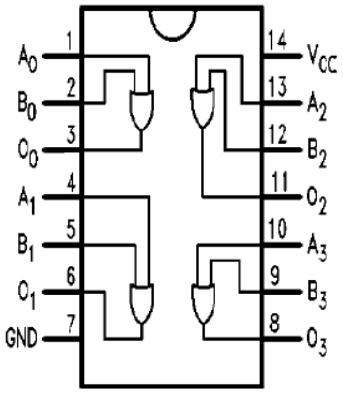
7408 (AND)



7486(EX-OR)



7432(OR)



SPECIFICATION OF APPARATIUS USED: Power Supply, Digital Trainer Kit., Connecting Leads, IC's (7400, 7402, 7404, 7408, 7432, and 7486)

PROCEDURE:

(a) Fix the IC's on breadboard & gives the supply.
(b) Connect the +ve terminal of supply to pin14 & -ve to pin7.
(c) Give input at pin1, 2 & take output from pin3.It is same for all except NOT & NOR IC.
(d) For NOR, pin1 is output & pin2&3 are inputs.
(e) For NOT, pin1 is input & pin2 is output.
(f) Note the values of output for different combination of inputs & draw the ckt

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

OBSERVATION DATA:

INPUTS		OUTPUTS					
A	B	A' NO	A+ BO	(A+B) 'NO	(A*B)AN	(A*B)' NAN	(A B)Ex-
0	0	1	0	1	0	1	0
0	1	1	1	0	0	1	1
1	0	0	1	0	0	1	1
1	1	0	1	0	1	0	0

RESULT AND COMMENTS: We have learn tall the gates ICs according to the IC pin diagram.

EXPERIMENT 2

AIM: Implementation of the Given Boolean Function using Logic Gates in Both Sop and Pos Forms.

THEORETICAL CONCEPT:-

Karnaugh maps are the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an n-variable K-map there are 2^n cells. Each cell corresponds to one of the combination of n variable, since there are 2^n combinations of n variables.

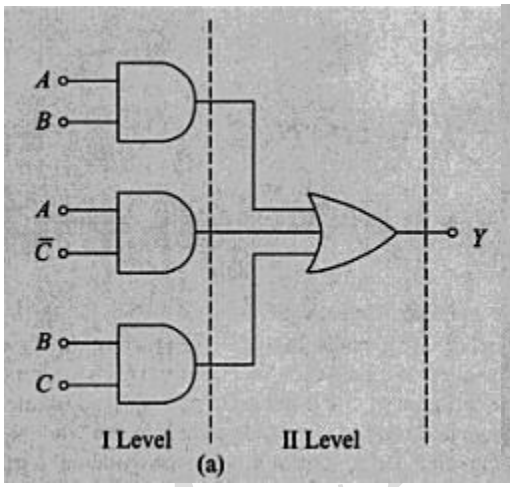
Gray code has been used for the identification of cells.

Example- SOP: $Y = AB + A\bar{C} + BC$

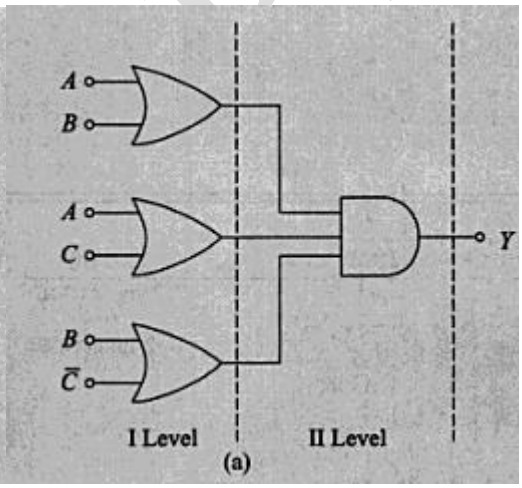
POS: $Y = (A+B)(A+C)(B+\bar{C})$

EXPERIMENTAL SET UP:-

SOP form



POS FORM



SPECIFICATION OF APPARATUS USED:- Power Supply, Digital Trainer, IC's (7404, 7408,7432) Connecting leads.

PROCEDURE:

(a) With given equation in SOP/POS forms first of all draw a Kmap.
(b) Enter the values of the O/P variable in each cell corresponding to its Min/Max term.
(c) Make group of adjacent ones.
(d) From group write the minimized equation.
(e) Design the ckt. of minimized equation & verify the truth table.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.

RESULT AND COMMENTS:-Implementation of SOP and POS form is obtained with AND and OR gates.

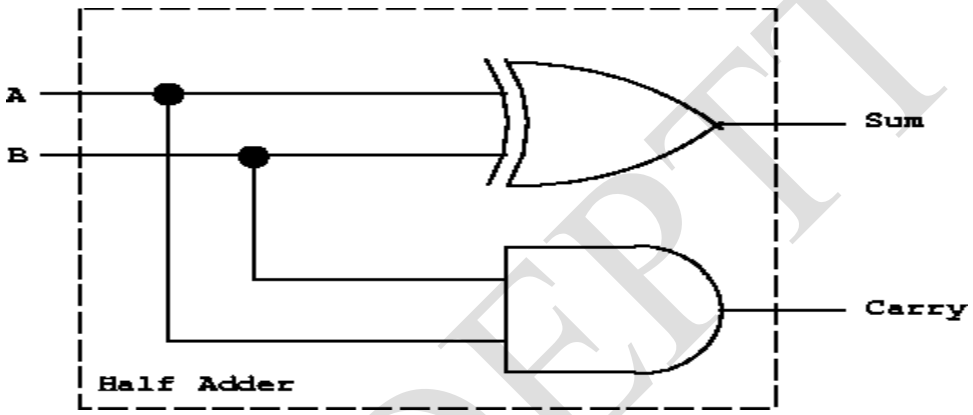
EXPERIMENT NO. 3

AIM:-To Study the Half Adder.

THEORETICAL CONCEPT:-

A half adder is a logic circuit that performs one-digit addition.
The half adder is an example of a simple, functional digital circuit built from logic gates. The half adder adds to one-bit binary numbers (AB). The output is the sum of the two bits (S) and the carry (C).

EXPERIMENTAL SET UP:-



SPECIFICATION OF APPARATUS USED:- I.C's 7486, 7408, wires, LED, Bread Board, 5 Volt supply.

PROCEDURE:-

1. Write OBSERVATION DATA for variables A, B. solves this OBSERVATION DATA with the help of K-map.
2. Connect the circuit as shown and get the output of Sum and Carry separately.
3. Firstly, we will put IC's.
4. Take input from Pin no. 1&2 of IC no.7486 and take output at Pin no.3.
5. Pin no.3 is connected with LED.
6. Short Pin no.1 of IC no.7486 to Pin no.2 of IC no.7408.
7. Similarly, short Pin no.1 of IC no.7486 to Pin no.1 of IC no.7408.
8. Take output at Pin no.3 of IC no.7408 and connect to LED.
9. Connect the Pin no. 14 to the 5 volt supply for all IC's used in the circuit.
10. Connect Pin no. 7 to ground for all the IC's

PRECAUTIONS:-

1. Supply should not exceed 5v.
2. Connections should be tight and easy to inspect.
3. Use L.E.D. with proper sign convention and check it before connecting in circuit.

OBSERVATION DATA:-

A	B	Sum	Carry
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

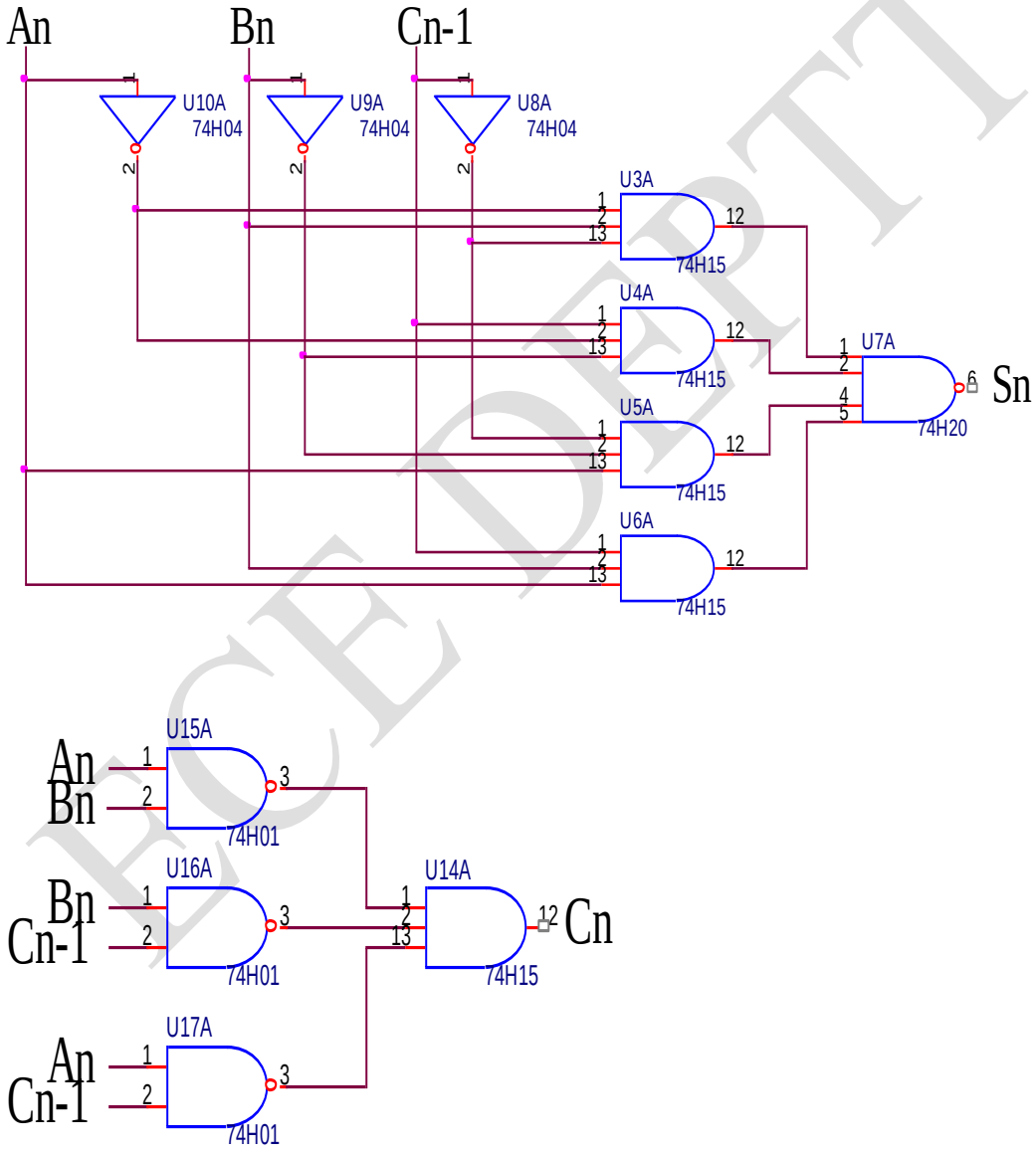
RESULT AND COMMENTS:- the observation data of half adder verified.

EXPERIMENT NO. 4

AIM:-To study about full adder & verify its observation data.

THEORETICAL CONCEPT:-An half adder has only two inputs and there is no provision to add a carry coming from the lower order bits when multibit addition is performed. For this purpose, a third input terminal is added and this circuit is used to add An, Bn and Cn-1 where An and Bn are the nth order bits of the numbers A and B respectively and Cn-1 is the carry generated from the addition of (n-1)th order bits. This circuit is referred to as FULL-ADDER.

EXPERIMENTAL SET UP:-



SPECIFICATION OF APPARATUS USED:-IC-(7486,7408,7432),Connecting wires, LED, Bread board,Cutter,5v supply.

PROCEDURE:

1. Write the OBSERVATION DATA for variables An, Bn and Cn-1.
2. OBSERVATION DATA was solved with the help of K-map.
3. Circuit was connected and the outputs of sum and carry was got separately.
4. Connect the pin no.14 to 5v supply of all IC's used in circuit.
5.Pin no. 7 will be grounded of all IC's.

PRECAUTIONS:-

1. Supply should not exceed 5v.
2. Connections should be tight and easy to inspect.
3. Use L.E.D. with proper sign convention and check it before connecting in circuit

OBSERVATION DATA:-

INPUTS			**OUTPUTS**	
An	Bn	Cn-1	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

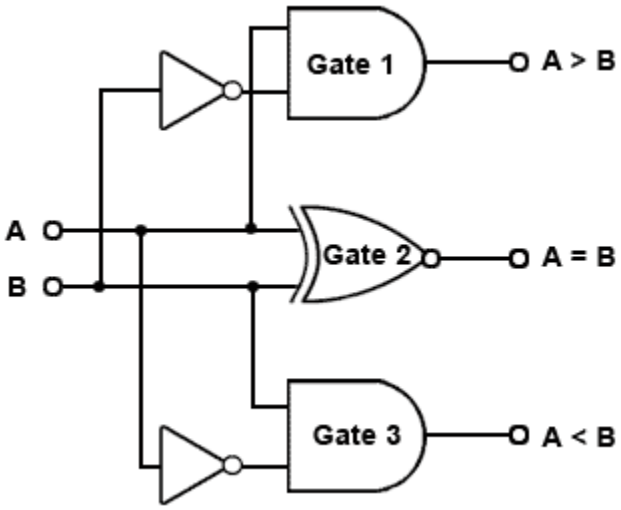
RESULT AND COMMENTS:- the observation data of full adder is verified.

EXPERIMENT NO. 5

AIM:-To Design & Verify the Operation of Magnitude Comparator

THEORETICAL CONCEPT:- Comparator compares the value of signal at the input. It can be designed to compare many bits. The adjoining figure shows the block diagram of comparator. Here it receives to two 2-bit numbers at the input & the comparison is at the output.

EXPERIMENTAL SET UP: - Comparator



SPECIFICATION OF APPARATUS USED:-

Power Supply , Digital Trainer Kit. Connecting Leads, and IC's (7404, 7408, and7486).

PROCEDURE:-

a. Make the connections according to the circuit diagram.
b. The output is high if both the input sare equal.
c. Verify the truth table for different values.

PRECAUTIONS:-

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only

OBSERVATION DATA:-

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

RESULT AND COMMENTS:- The comparator is designed & verified.

EXPERIMENT NO : 6

AIM:- Implementation of 4x1 Multiplexer and 1x4 Demultiplexer using Logic Gates.

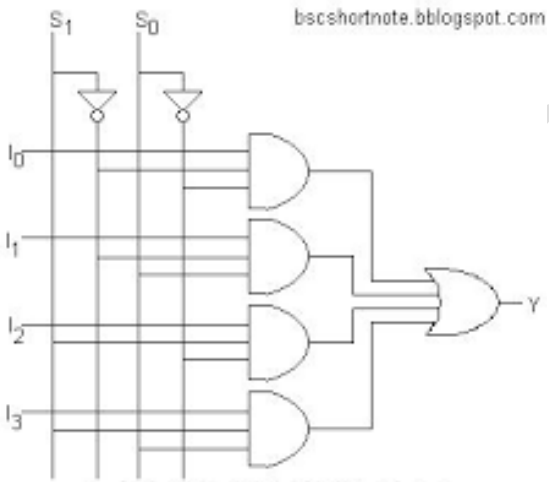
THEORETICAL CONCEPT:-

MULTIPLEXER: Multiplexer generally means many into one. A multiplexer is a circuit with many Inputs but only one output. By applying control signals we can steer any input to the output .The fig. (1) Shows the general idea. The ckt. has n-input signal,control signal & one output signal. Where 2n = m. One of the popular multiplexer is the 4 to 1 multiplexer, which has 4 input bits, 2 control bits & 1 output bit.

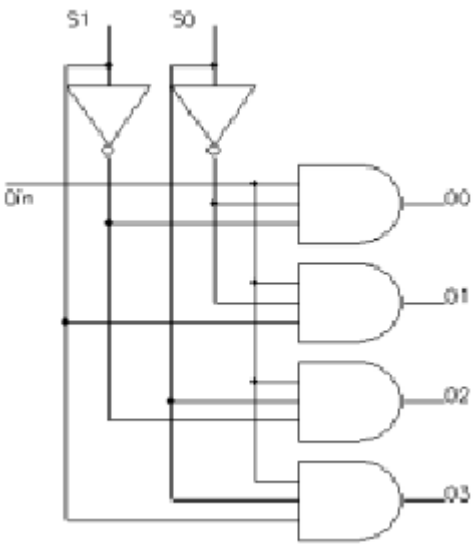
DEMULTIPLEXER: Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many outputs. By applying control signals, we can steer the input signal to one of the output lines. The ckt. has one input signal, m control signal and n output signals. Where 2n = m. It functions as an electronic switch to route an incoming data signal to one of several outputs

EXPERIMENTAL SET UP: -

Multiplexer (4x1) Demultiplexer (1x4)



CIRCUIT DIAGRAM OF 4X1 MUX USING LOGIC GATES



SPECIFICATION OF APPARATUS USED:-

Power Supply, Digital Trainer, Connecting Leads, IC's74153(4x1 multiplexer).

PROCEDURE:

1) Connect the circuit as shown in figure.
2) Apply Vcc & ground signal to every IC.
3) Observe the input & output according to the truth table.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.

OBSERVATION DATA:

Truth table for Mux

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Truth table for Demux

Output select Lines		Output selected
S_1	S_0	
0	0	O_0
0	1	O_1
1	0	O_2
1	1	O_3

RESULT AND COMMENTS:

Verify the truth table of multiplexer and demultiplexer for various inputs.

EXPERIMENT NO. 7

AIM: Verification of State Tables of Rs ,J-k ,T and D Flip-Flops using NAND Gates

THEORETICAL CONCEPT:-

•RS FLIP-FLOP: There are two inputs to the flip-flop defined as R and S . When I/Ps R=0 and S=0 then O/P remains unchanged .When I/Ps R=0andS=1 the flip-flop is switches to the stable state where O/P is 1i.e. SET. The I/P condition is R=1 and S=0 the flip-flop is switched to the stable state where O/P is 0i.e. RESET. The I/P condition is R=1 and S=1 the flip-flop is switched to the stable state where O/P is forbidden.

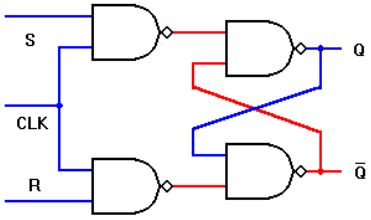
•JK FLIP-FLOP: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both0s, both AND gates are disabled and Q retain sits last value.

•D FLIP–FLOP: This kind of flipflop preventsthevalueofDfromreachingtheQoutputuntilclockpulsesoccur.Whentheclockislow,bothANDgatesaredisabledDcanchangevaluewithoutaffectingthevalueofQ.Ontheotherhand, whentheclockishigh,bothANDgatesareenabled.Inthiscase,Qisforcedtoequalthevalueof D. Whentheclockagaingoeslow,Qretainsorstoresthelastvalueof D.aDflipflopisabistablecircuit whoseDinputistransferredtotheoutputafteraclockpulseisreceived.

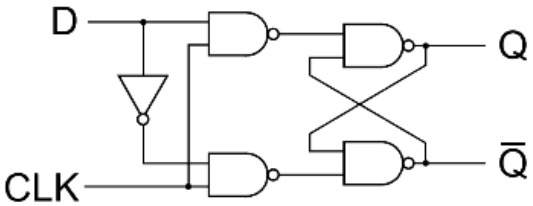
•T FLIP-FLOP:TheTor"toggle"flip-flopchangesitsoutputoneachclockedge,givinganoutputwhichishalfthefrequencyofthesignal totheTinput.It is usefulforconstructingbinarycounters,frequencydividers,andgeneralbinaryadditiondevices. ItcanbemadefromaJ-Kflip-flopbytyingbothofitsinputshigh.

EXPERIMENTAL SET UP: -

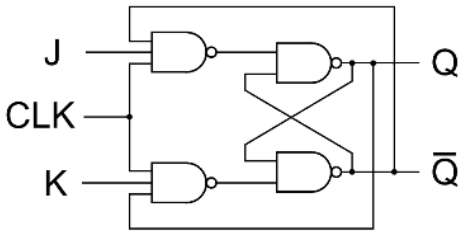
SRFlipFlop



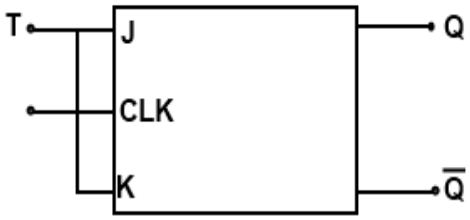
DFlipFlop



JK FLIP FLOP



T FLIP FLOP



SPECIFICATION OF APPARATUS USED:- IC' S 7400, 7402 Digital Trainer & Connecting leads.

PROCEDURE:

1. Connect the circuit as shown in figure.
2. Apply Vcc & ground signal to every IC.
3. Observe the input & output according to the truth table.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only

OBSERVATION DATA:-

TRUTHTABLE:SRFLIP FLOP:

SR FLIP FLOP:-

CLOCK	S	R	Q
1	**0**	**0**	**NOCHANGE**
1	**0**	**1**	**0**
1	**1**	**0**	**1**
1	**1**	**1**	**?**

D FLIP FLOP:-

CLOCK	D	Q
1	**0**	**0**
1	**1**	1

JK FLIP FLOP:-

CLOCK	J	K	Q
1	**0**	**0**	**NOCHANGE**
1	**0**	**1**	**0**
1	**1**	**0**	**1**
1	**1**	**1**	**Q'**

T FLIP FLOP:-

CLOCK	T	Q
1	0	NOCHANGE
1	1	Q′

RESULT AND COMMENT:-Truth table is verified on digital trainer.

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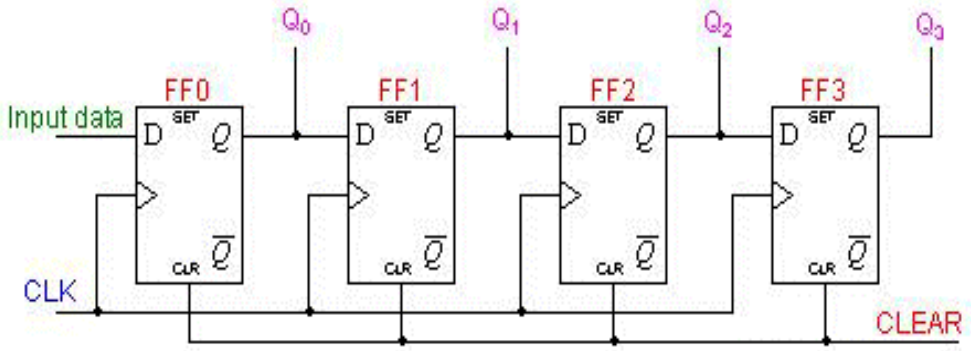
EXPERIMENT NO. 8

Aim: – Design, and Verify the 4-Bit Serial In - Parallel Out Shift Registers.

THEORETICAL CONCEPT:-shift register is used to shift the data there 4 type of shift register: siso,sipo,piso,pipo. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below

EXPERIMENTAL SET UP: -



SPECIFICATION OF APPARATUS USED:- Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

OBSERVATION DATA:-
TRUTH TABLE:

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

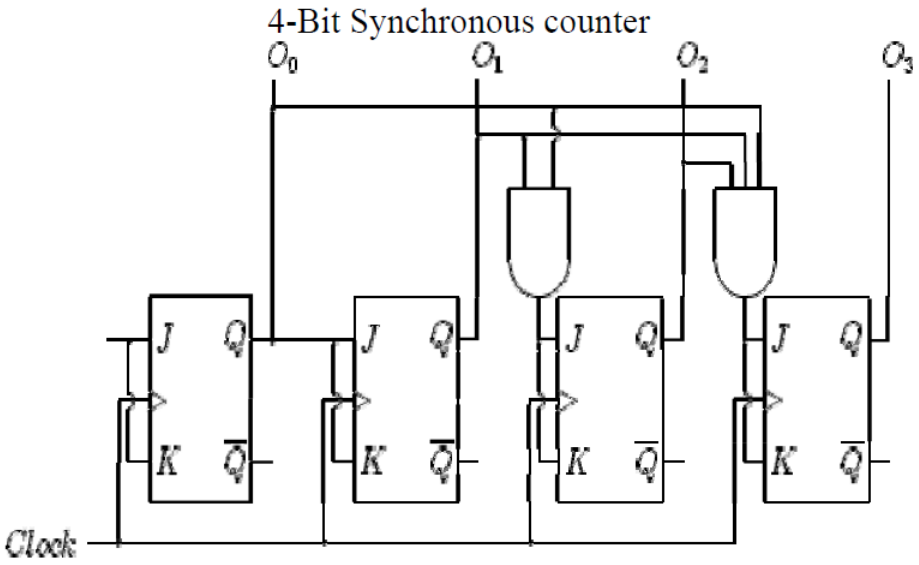
RESULT AND COMMENT: 4-bit Serial In – Parallel Out Shift Registers studied and verified.

EXPERIMENTNO:9

Aim:–Design ,and Verify the 4-Bit Synchronous Counter

THEORETICAL CONCEPT:-
Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter(e.g. parallel) and Asynchronous counter(e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

EXPERIMENTAL SET UP: -



SPECIFICATION OF APPARATUS USED:- Digital trainer kit and 4 JK flip flop each IC7476 (i.e dual JK flip flop)andtwoANDgatesIC7408.

OBSERVATION DATA:

TRUTH TABLE

States				Count
0_4	0_3	0_2	0_1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

RESULT AND COMMENT: 4-bit synchronous counter studied and verified.

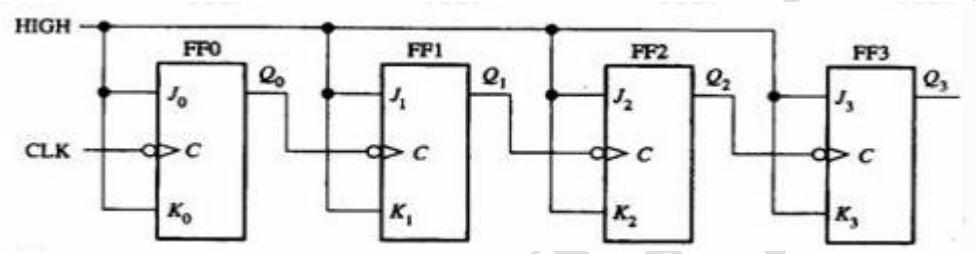
EXPERIMENT NO: 10

Aim: – Design, and Verify the 4-Bit Asynchronous Counter.

THEORETICAL CONCEPT:-Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

EXPERIMENTAL SET UP: -

4-Bit Asynchronous counter



SPECIFICATION OF APPARATUS USED:- Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

RESULT AND COMMENT: 4-bit asynchronous counter studied and verified.